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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,700	12/07/2001	Hong-Sik Jeong	5649-905	5150

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MYERS BIGEL SIBLEY & SAJOVEC  
PO BOX 37428  
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EXAMINER
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LUU, CHUONG A

ART UNIT	PAPER NUMBER
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2818

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/14/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

**Office Action Summary**

Application No.

10/008,700

Applicant(s)

JEONG ET AL.

Examiner

Chuong A. Luu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 22 January 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 6-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 6-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Response to Arguments***

Applicant's arguments with respect to claims 6-24 have been considered but are moot in view of the new ground(s) of rejection.

## **PRIOR ART REJECTIONS**

### **Statutory Basis**

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

### **The Rejections**

Claims 6, 10, 12-13, 15, 17-18, 21 and 24 rejected under 35 U.S.C. 102(b) as being anticipated by Chen (U.S. 6,078,073).

Chen discloses a gate electrode structure with.

(6); (15) forming a pattern comprising a pair of mesa regions (7) on a substrate (5) (see Figure 1);

forming a first insulating layer (11) on the pair of mesa regions (7) (see Figure 1);

forming a second insulating layer (13) on the pair of mesa regions (7) and the substrate (5) (see Figure 1);

forming a capping layer (15) on the second insulating layer (13) (see Figure 1);

patterning the capping layer (15) and the second insulating layer (13) together, such that parts of the first insulating layer (11) that were covered by the second insulating layer (13) are exposed without exposing the mesa regions (7) under the first insulating layer (11) (see Figure 2);

forming insulating spacers (21) on sidewalls of the second insulating layer (13) such that the second insulating layer (13) is enclosed by the insulating spacers (21), the capping layer (15), the first insulating layer (11), and the substrate (5) (see Figure 3);

(10); (21) further comprising: forming a conductive layer on the pair of mesa regions and the substrate so as to fill a contact region between the pair of mesa regions and to cover the mesa regions; removing a portion of the conductive layer such that an upper surface of the first insulating layer, opposite the substrate, is exposed (see Figure 6);

(12); (24) wherein the capping layer may comprise at least one of silicon oxide, silicon nitride (see column 2, lines 65-66);

(13); (17) wherein forming the insulating spacers comprises: forming a third insulating layer on the capping layer, the sidewalls of the second insulating layer, and the substrate; etching the third insulating layer so as to remove at least a portion of the third insulating layer from the substrate and an upper surface of the capping layer, opposite the substrate (see Figures 2-3).

(18) further comprising: removing at least a portion of the etch stop layer from a contact region between the pair of mesa regions (see Figures 3-4).

## **PRIOR ART REJECTIONS**

### **Statutory Basis**

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

### **The Rejections**

Claims 7-9, 14, 16, 19-20 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (U.S. 6,078,073) in view of Takagi et al. (U.S. 5,072,282).

Chen discloses the claimed invention except for specifically describing wherein each of the insulating spacers has a width in a range of about 50Å to about 200Å; wherein the cleaning solution comprises at least one of hydrofluoric (HF) acid and wherein the second insulating layer is a spin on glass layer. However, Takagi discloses a semiconductor device with (7); (16) wherein the second insulating layer is a spin on glass layer (see column 7, lines 19-26); (8); (19) further comprising: applying a cleaning solution to the integrated circuit device so as to expose a contact region between the pair of mesa regions by removing at least a portion of a native oxide layer from the contact region (see column 1, lines 20-27); (9); (20) wherein the cleaning solution comprises at least one of hydrofluoric (HF) acid (see column 1, lines 20-27). Even though, Chen and Takagi do not explicitly describe wherein each of the insulating spacers has a width in a range of about 50Å to about 200Å. However, the insulating

spacers has a width in a range of about 50Å to about 200Å is considered to be obvious. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teaching of Chen (accordance with the teaching of Takagi) since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice, and it also has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art and it is noted that the applicant does not disclose criticality in the ranges claimed. In re Leshin, 125 USPQ 416 and In re Aller, 105 USPQ 233 (see MPEP 2144.05). Doing so would facilitate the manufacture of the semiconductor device and increase the speed of the semiconductor structure.

Claims 11 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (U.S. 6,078,073) in view of Dennison (U.S. 5,401,681).

Chen teaches everything above except for wherein removing the portion of the conductive layer comprises: chemical mechanical polishing the conductive layer such that the upper surface of the first insulating layer, opposite the substrate, is exposed. However, Dennison discloses a semiconductor device with (11); (22) wherein removing the portion of the conductive layer comprises: chemical mechanical polishing the conductive layer such that the upper surface of the first insulating layer, opposite the substrate, is exposed (see column 6, lines 55-60). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to

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modify the teaching of Chen by applying the chemical mechanical polishing process, which is a well-known in the art, to remove a conductive material as taught by Dennison.

**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Chuong Anh Luu  
Patent Examiner  
June 30, 2006